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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/727,272 | 12/03/2003 | Chung-Yi Yu | 24061.25 | 4831 |

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| EXAMINER | |
|---|---|
| KENNEDY, JENNIFER M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/727,272 | YU ET AL. | |
| | Examiner | Art Unit | |
| | Jennifer M. Kennedy | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *19-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 26-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election with traverse of Group I and claims 1-18, and 25-26, in the reply filed on May 12, 2005 is acknowledged. The traversal is on the ground(s) that the embodiments are not patentable distinct. This is not found persuasive because the examiner has demonstrated why the subject matter is distinct in the restriction requirement mailed February 3, 2005 by stating:

The inventions are distinct, each from the other because:

Inventions III and IV are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not require the step of coupling the substrate to a rotatable polishing head. The subcombination has separate utility such as in a method wherein selective deposition is used in lieu of a mask and etch process. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, the search required for Group IV is not required for Group III, and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

The requirement is still deemed proper and is therefore made FINAL.

Claims 19-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on May 12, 2005.

***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on February 9, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

***Claim Objections***

Claim 17 is objected to because of the following informalities: The claim recites that the "planarizing pressure ranging of at least 5.0 psi." is grammatically incorrect. The examiner suggests amending the claim to recite "planarizing pressure of at least 5.0 psi". Appropriate correction is required.

***Misnumbered Claims***

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 25 (second occurrence) and claim 26 have been renumbered 26 and 27 respectively. The examiner notes the dependency of claim 27 should be changed, and request applicant's cooperation in amending.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 10-14, 18, and 26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (U.S. Patent No. 6,855,602).

In re claim 1, Chang et al. disclose a method of manufacturing a semiconductor device, comprising:

forming a gate structure (12A, 12B) over a substrate (10);

forming an interconnect layer (23A) over the gate structure and the substrate;

forming a cap layer (23B) over the interconnect layer;

planarizing the interconnect layer and the cap layer to form a substantially planar surface, the substantially planar surface having a portion of exposed interconnect layer and a portion of exposed cap layer (see column 4, lines 47-57, and Figure 1C);

forming a mask layer over the exposed portion of the planarized interconnect layer (24A, see column 5, lines 20-40; and Figure 1E);

removing material underlying the exposed portion of the planarized cap layer (see Figure 1F and 1G and column 5, lines 40-55).

In re claim 2, Chang et al. disclose the method wherein the interconnect layer is formed over the gate structure to a thickness that is less than a height of the gate structure (see Figure 1A).

In re claim 3, Chang et al. disclose the method wherein the mask layer is formed by an anneal process (see column 5, lines 20-40).

In re claim 4, Chang et al. disclose the method further comprising removing the mask layer after removing the planarized cap layer (see Figure 1F and 1G and column 5, lines 40-55).

In re claim 5 and 6, Chang et al. disclose the method wherein a first removal rate of the interconnect layer during the planarizing is greater than a second removal rate of the cap layer during the planarizing and wherein the first removal rate is at least three times greater than the second removal rate. While Chang et al. does not explicitly disclose this relationship the examiner notes that Applicants state in the specification at [0030] that "Because polysilicon is about three times as resistant to CMP as $Si_3N_4$, a polishing rate ratio of about 3:1 or about 5:1 may be achieved." Therefore, since Chang et al. uses a polysilicon interconnect layer and a cap layer of $Si_3N_4$, the removal rate in Chang et al. the first removal rate of the interconnect layer during the planarizing is at

least three times greater than a second removal rate of the cap layer during the planarizing.

In re claim 7, Chang et al. disclose the method wherein the cap layer (23B) is formed directly on the interconnect layer (23A, see Figure 1B).

In re claim 8, Chang et al. disclose the wherein a portion of the cap layer is separated from the substrate by a distance that is less than the height of the gate structure (see Figure 1B).

In re claim 10, Chang et al. disclose the method wherein the cap layer comprises $Si_3N_4$ (see column 4, lines 12-15).

In re claim 11, Chang et al. disclose the method wherein the mask layer comprises $SiO_2$ (see column 5, lines 20-40).

In re claim 12, Chang et al. disclose the method wherein removing material includes removing the cap layer and removing polysilicon (see Figure 1F and 1G and column 5, lines 40-55).

In re claim 13, Chang et al. disclose the method wherein the cap layer has a thickness ranging between 100 angstroms and 2000 angstroms before planarizing (see column 4, lines 12-26).

In re claim 14, Chang et al. disclose the method wherein the planarizing includes chemical-mechanical polishing (see column 4, lines 47-57, and Figure 1C).

In re claim 18, Chang et al. disclose the method wherein the device is a split gate field effect transistor (see column 2, lines 60-65).

In re claim 26, Chang et al. disclose the method of forming a box-shaped interconnect, comprising:

forming an interconnect layer (23A) above and beside an electrode structure (12A, 12B);

forming a cap layer (23B) over the interconnect layer;

planarizing the cap layer and interconnect layer to leave an exposed portion of the interconnect layer and a capped portion of the interconnect layer (see column 4, lines 47-57, and Figure 1C);

forming a hard mask over the exposed portion of the interconnect layer (24A, see column 5, lines 20-40; and Figure 1E); and

removing the capped portion of the interconnect layer(see Figure 1F and 1G and column 5, lines 40-55).

In re claim 27, Chang et al. disclose the method wherein the electrode structure is a split gate (see column 2, lines 60-65).

Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (U.S. Patent Appl. 2004/0171243).

In re claim 1, Lee et al. disclose a method of manufacturing a semiconductor device, comprising:

forming a gate structure (110) over a substrate (200);

forming an interconnect layer (130) over the gate structure and the substrate;

forming a cap layer (150) over the interconnect layer;

planarizing the interconnect layer and the cap layer to form a substantially planar surface, the substantially planar surface having a portion of exposed interconnect layer and a portion of exposed cap layer (see Figure 5F and paragraphs [0062] and [0063]);

forming a mask layer over the exposed portion of the planarized interconnect layer (125, see Figure 5G and paragraph [0064]);

removing material underlying the exposed portion of the planarized cap layer (see Figures 5H and 5I and [0065] and [0066]).

In re claim 9, Chang et al. disclose the method wherein the cap layer comprises $SiO_2$ (see paragraph [0061]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,855,602) in view of Quek et al. (U.S. Patent No. 6,136,710).

In re claims 15-17, Chang et al. disclose the method as claimed and rejected above including the method wherein the CMP is utilized to planarize the interconnect and the cap layer, but does not disclose the method the polishing head speed ranges

between 75 rpm and 200 rpm and wherein the platen speed ranges between 65 rpm and 150 rpm and the planarizing pressure applied of at least 5.0 psi.

Quek et al. discloses the method of utilizing a polishing method including polishing head speed ranges between 75 rpm and 200 rpm and wherein the platen speed ranges between 65 rpm and 150 rpm and the planarizing pressure applied of at least 5.0 psi (see column 6, lines 10-21) it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a polishing method with polishing head speed ranges between 75 rpm and 200 rpm, platen speed ranges between 65 rpm and 150 rpm, planarizing pressure applied of at least 5.0 psi, because as Quek et al. teaches the method allows for polishing uniformity on the substrate (see abstract and column 2, lines 65 through column 3, line 2).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cho et al. (U.S. Patent Appl. 2003/0113969), Kim et al. (U.S. Patent No. 6,524,915), Cho et al. (U.S. Patent Appl. 2003/0022442), Cho et al. (U.S. Patent Appl. 2004/0156247), and Wang (U.S. Patent Appl. (2003/0139010) disclose methods similar to that of the claimed method. Tsai et al. (U.S. Patent No. 5,575,706) disclose the claimed ranges of polishing speed and pressure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk